

# EMS42CHE-36.975M

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## REGULATORY COMPLIANCE (Data Sheet downloaded on Dec 5, 2019)


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## ITEM DESCRIPTION

Spread Spectrum MEMS Clock Oscillators LVCMOS (CMOS) 2.5Vdc 4 Pad 2.0mm x 2.5mm Plastic Surface Mount (SMD) 36.975MHz  $\pm$ 100ppm Maximum over -20°C to +70°C Tri-State -1.00% Down Spread

## ELECTRICAL SPECIFICATIONS

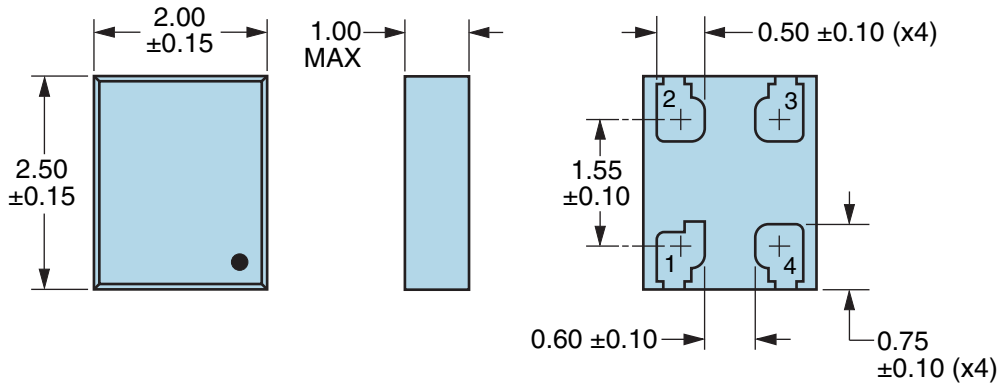
Nominal Frequency	36.975MHz
Frequency Tolerance/Stability	$\pm$ 100ppm Maximum over -20°C to +70°C (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, 260°C Reflow, Shock, and Vibration)
Aging at 25°C	$\pm$ 1ppm Maximum First Year
Supply Voltage	2.5Vdc $\pm$ 10%
Maximum Supply Voltage	-0.5Vdc to +3.65Vdc
Input Current	35mA Maximum (Unloaded; Nominal Vdd)
Output Voltage Logic High (Voh)	90% of Vdd Minimum (IOH=-8mA)
Output Voltage Logic Low (Vol)	10% of Vdd Maximum (IOL=+8mA)
Rise/Fall Time	2nSec Maximum (Measured from 20% to 80% of waveform)
Duty Cycle	50 $\pm$ 5(%) (Measured at 50% of waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Output Control Function	Tri-State (Disabled Output High Impedance)
Tri-State Input Voltage (Vih and Vil)	70% of Vdd Minimum or No Connection to Enable Output, 30% of Vdd Maximum to Disable Output
Disable Current	20mA Maximum (Disabled Output: High Impedance) (Pad 1=Ground)
Spread Spectrum	-1.00% Down Spread
Modulation Frequency	30kHz Minimum, 32kHz Typical, 35kHz Maximum
Period Jitter	40pSec Maximum (Cycle to Cycle; Spread Spectrum-On; Fo=133.333M, Vdd=2.5Vdc)
Start Up Time	10mSec Maximum
Storage Temperature Range	-55°C to +125°C

## ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

ESD Susceptibility	MIL-STD-883, Method 3015, Class 2, HBM 2000V
Flammability	UL94-V0
Mechanical Shock	MIL-STD-883, Method 2002, Condition G, 30,000G
Moisture Resistance	MIL-STD-883, Method 1004
Moisture Sensitivity Level	J-STD-020, MSL 1
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003 (Pads on Bottom of Package Only)
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Thermal Shock	MIL-STD-883, Method 1011, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A, 20G

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### MECHANICAL DIMENSIONS (all dimensions in millimeters)



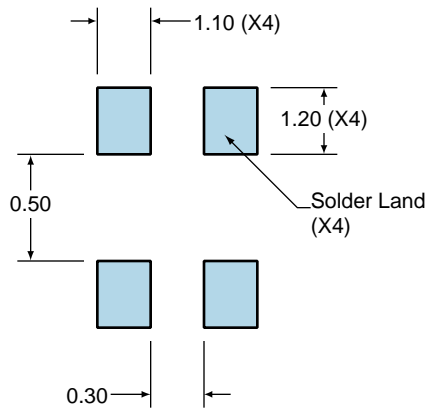
PIN	CONNECTION
1	Tri-State (High Impedance)
2	Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	<b>XXXX or XXXXX</b> XXXX or XXXXX=Ecliptek Manufacturing Identifier

### Suggested Solder Pad Layout

All Dimensions in Millimeters



All Tolerances are  $\pm 0.1$

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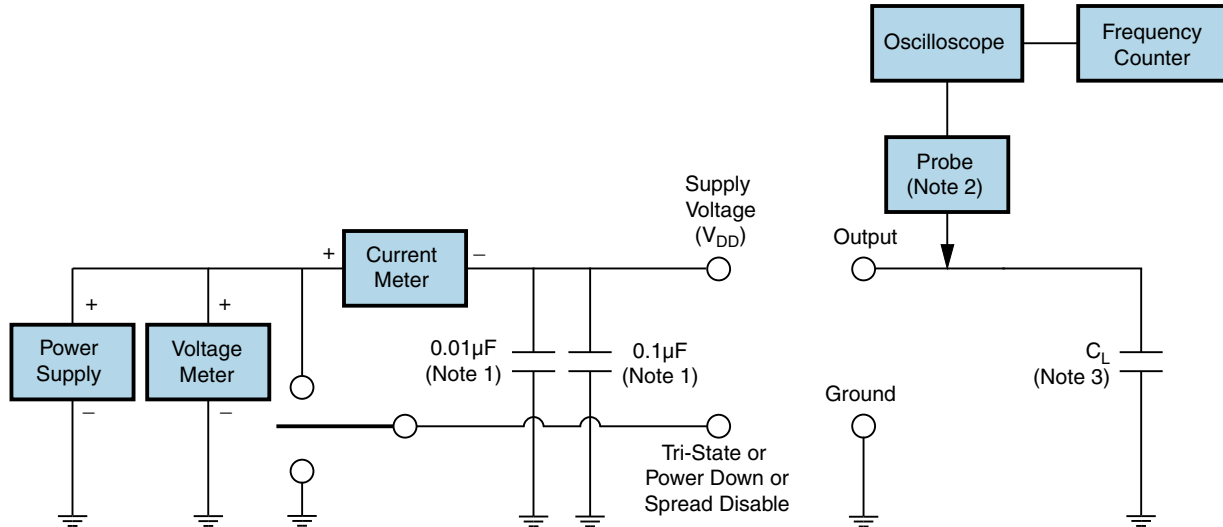
## OUTPUT WAVEFORM & TIMING DIAGRAM



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## Test Circuit for CMOS Output



Note 1: An external  $0.01\mu\text{F}$  ceramic bypass capacitor in parallel with a  $0.1\mu\text{F}$  high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low capacitance ( $<12\text{pF}$ ), 10X attenuation factor, high impedance ( $>10\text{Mohms}$ ), and high bandwidth ( $>300\text{MHz}$ ) passive probe is recommended.

Note 3: Capacitance value  $C_L$  includes sum of all probe and fixture capacitance.