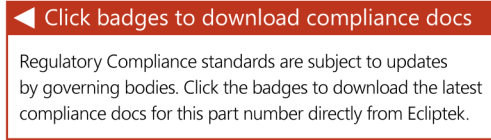


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REGULATORY COMPLIANCE (Data Sheet downloaded on Nov 12, 2019)



ITEM DESCRIPTION

Spread Spectrum Quartz Crystal Clock Oscillators LVCMOS (CMOS) 2.5Vdc 4 Pad 3.2mm x 5.0mm Ceramic Surface Mount (SMD) 84.111235MHz ± 50 ppm Maximum -40°C to +85°C Power Down -0.50% Down Spread

ELECTRICAL SPECIFICATIONS

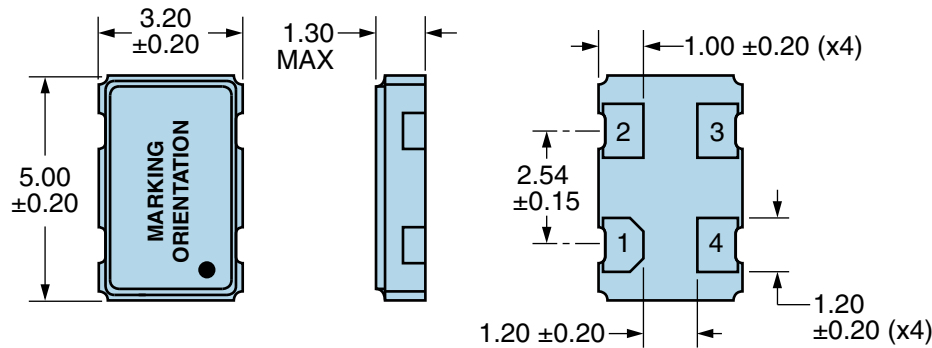
Nominal Frequency	84.111235MHz
Frequency Tolerance/Stability	± 50 ppm Maximum (Inclusive of all conditions: Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration.)
Operating Temperature Range	-40°C to +85°C
Supply Voltage	2.5Vdc $\pm 5\%$
Maximum Supply Voltage	-0.5Vdc to +3.2Vdc
Input Current	22mA Maximum
Output Voltage Logic High (Voh)	90% of Vdd Minimum (IOH=-8mA)
Output Voltage Logic Low (Vol)	10% of Vdd Maximum (IOL=+8mA)
Rise/Fall Time	3nSec Maximum (Measured at 10% to 90% of Waveform)
Duty Cycle	50 ± 5 (%) (Measured at 50% of waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Output Control Function	Power Down (Disabled Output: High Impedance)
Power Down Input Voltage (Vih and Vil)	70% of Vdd Minimum or No Connection to Enable Output, 30% of Vdd Maximum to Disable Output
Power Down Output Enable Time	3mSec Maximum
Power Down Output Disable Time	100nSec Maximum
Standby Current	10 μ A Maximum (Unloaded; Pad 1=Ground)
Spread Spectrum	-0.50% Down Spread
Modulation Frequency	30kHz Minimum, 32kHz Typical, 45kHz Maximum
Period Jitter	100pSec Maximum (Cycle to Cycle; Spread Spectrum-On)
Start Up Time	10mSec Maximum
Storage Temperature Range	-55°C to +125°C

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

ESD Susceptibility	MIL-STD-883, Method 3015, Class 1, HBM: 1500V
Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Flammability	UL94-V0
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Moisture Resistance	MIL-STD-883, Method 1004
Moisture Sensitivity	J-STD-020, MSL 1
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A

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MECHANICAL DIMENSIONS (all dimensions in millimeters)



PIN	CONNECTION
1	Power Down
2	Case/Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	E84.111 E=Ecliptek Designator
2	XXXXX XXXXX=Ecliptek Manufacturing Identifier

Suggested Solder Pad Layout

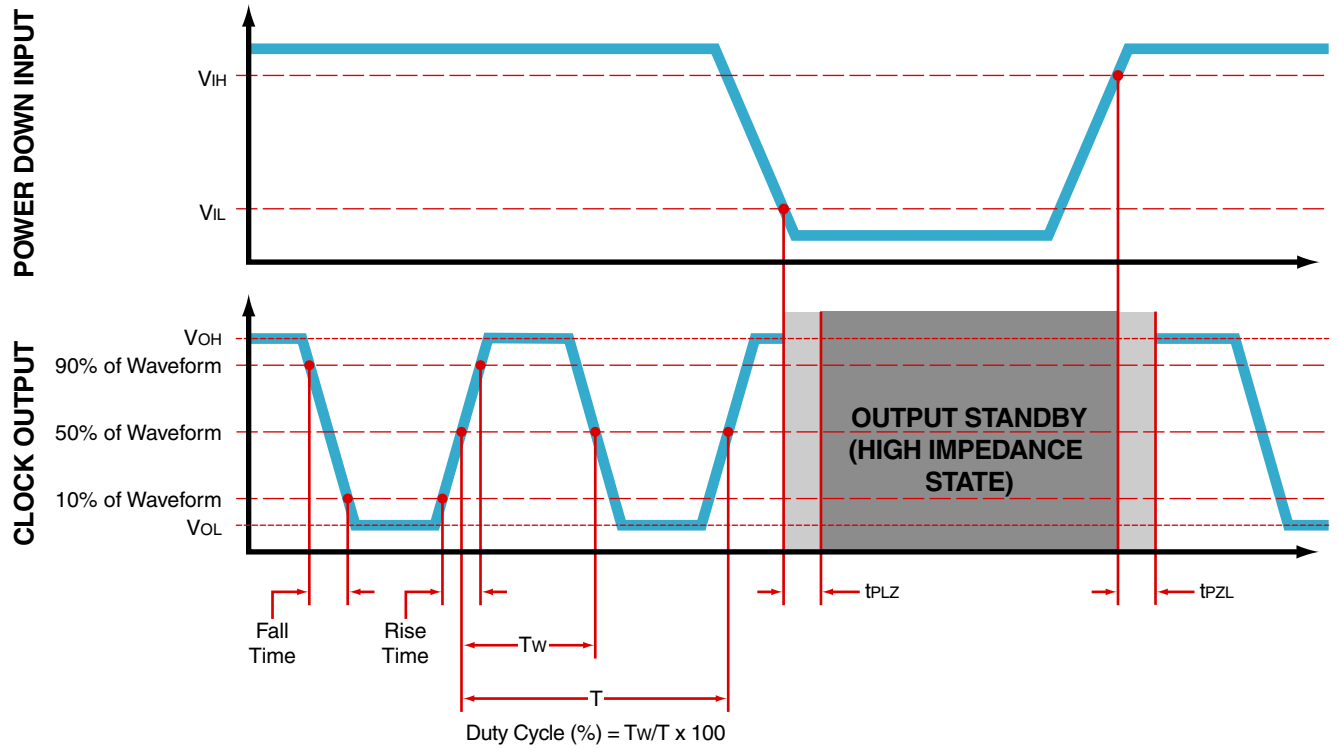
All Dimensions in Millimeters



All Tolerances are ± 0.1

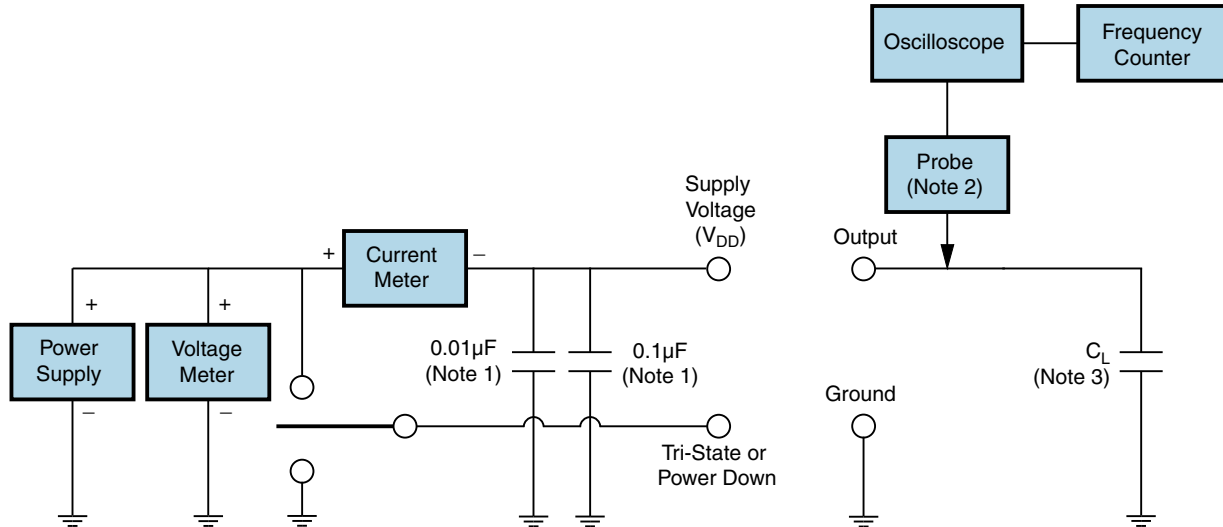
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OUTPUT WAVEFORM & TIMING DIAGRAM



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Test Circuit for CMOS Output



Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low input capacitance (<12pF), 10X Attenuation Factor, High Impedance (>10Mohms), and High bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value CL includes sum of all probe and fixture capacitance. See applicable specification sheet for 'Load Drive Capability'.