

# EPSA23BBHP-41.360M [Click part number to visit Part Number Details page](#)

## REGULATORY COMPLIANCE (Data Sheet downloaded on Apr 5, 2020)



◀ Click badges to download compliance docs

Regulatory Compliance standards are subject to updates by governing bodies. Click the badges to download the latest compliance docs for this part number directly from Ecliptek.



## ITEM DESCRIPTION

Spread Spectrum Quartz Crystal Clock Oscillators LVCMOS (CMOS) 3.3Vdc 4 Pad 3.2mm x 5.0mm Ceramic Surface Mount (SMD) 41.360MHz ±50ppm Maximum -40°C to +85°C Tri-State -4.00% Down Spread

## ELECTRICAL SPECIFICATIONS

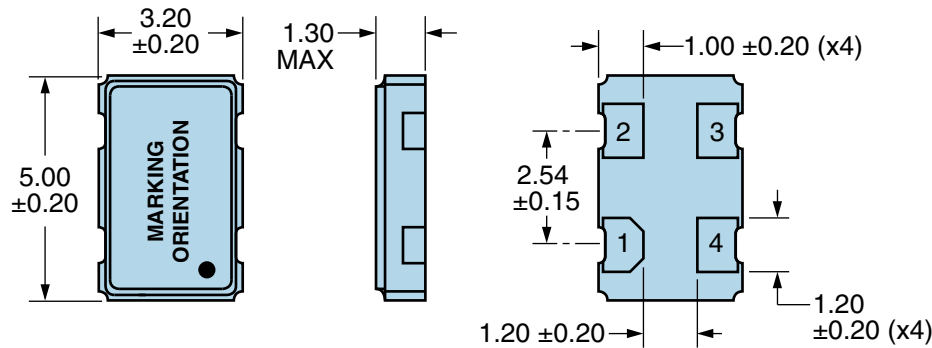
|                                       |  |
|---------------------------------------|--|
| Nominal Frequency                     | 41.360MHz  |
| Frequency Tolerance/Stability         | ±50ppm Maximum (Inclusive of all conditions: Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration.) |
| Operating Temperature Range           | -40°C to +85°C   |
| Supply Voltage                        | 3.3Vdc ±10%  |
| Maximum Supply Voltage                | -0.5Vdc to +4.2Vdc   |
| Input Current                         | 23mA Maximum   |
| Output Voltage Logic High (Voh)       | 90% of Vdd Minimum (IOH=-8mA)  |
| Output Voltage Logic Low (Vol)        | 10% of Vdd Maximum (IOL=+8mA)  |
| Rise/Fall Time                        | 3nSec Maximum (Measured at 10% to 90% of Waveform)   |
| Duty Cycle                            | 50 ±5(%) (Measured at 50% of waveform)   |
| Load Drive Capability                 | 15pF Maximum   |
| Output Logic Type                     | CMOS   |
| Output Control Function               | Tri-State (Disabled Output: High Impedance)  |
| Tri-State Input Voltage (Vih and Vil) | 70% of Vdd Minimum or No Connection to Enable Output, 30% of Vdd Maximum to Disable Output   |
| Tri-State Output Enable Time          | 100nSec Maximum  |
| Tri-State Output Disable Time         | 100nSec Maximum  |
| Disable Current                       | 20mA Maximum (Unloaded; Pad 1=Ground)  |
| Spread Spectrum                       | -4.00% Down Spread   |
| Modulation Frequency                  | 30kHz Minimum, 32kHz Typical, 45kHz Maximum  |
| Period Jitter                         | 100pSec Maximum (Cycle to Cycle; Spread Spectrum-On)   |
| Start Up Time                         | 10mSec Maximum   |
| Storage Temperature Range             | -55°C to +125°C  |

## ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

|                              |   |
|------------------------------|---|
| ESD Susceptibility           | MIL-STD-883, Method 3015, Class 1, HBM: 1500V |
| Fine Leak Test               | MIL-STD-883, Method 1014, Condition A         |
| Flammability                 | UL94-V0                                       |
| Gross Leak Test              | MIL-STD-883, Method 1014, Condition C         |
| Mechanical Shock             | MIL-STD-883, Method 2002, Condition B         |
| Moisture Resistance          | MIL-STD-883, Method 1004                      |
| Moisture Sensitivity         | J-STD-020, MSL 1                              |
| Resistance to Soldering Heat | MIL-STD-202, Method 210, Condition K          |
| Resistance to Solvents       | MIL-STD-202, Method 215                       |
| Solderability                | MIL-STD-883, Method 2003                      |
| Temperature Cycling          | MIL-STD-883, Method 1010, Condition B         |
| Vibration                    | MIL-STD-883, Method 2007, Condition A         |

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### MECHANICAL DIMENSIONS (all dimensions in millimeters)



| PIN | CONNECTION     |
|-----|----------------|
| 1   | Tri-State      |
| 2   | Case/Ground    |
| 3   | Output         |
| 4   | Supply Voltage |

| LINE | MARKING   |
|------|---|
| 1    | <b>E41.360</b><br>E=Ecliptek Designator                 |
| 2    | <b>XXXXX</b><br>XXXXX=Ecliptek Manufacturing Identifier |

### Suggested Solder Pad Layout

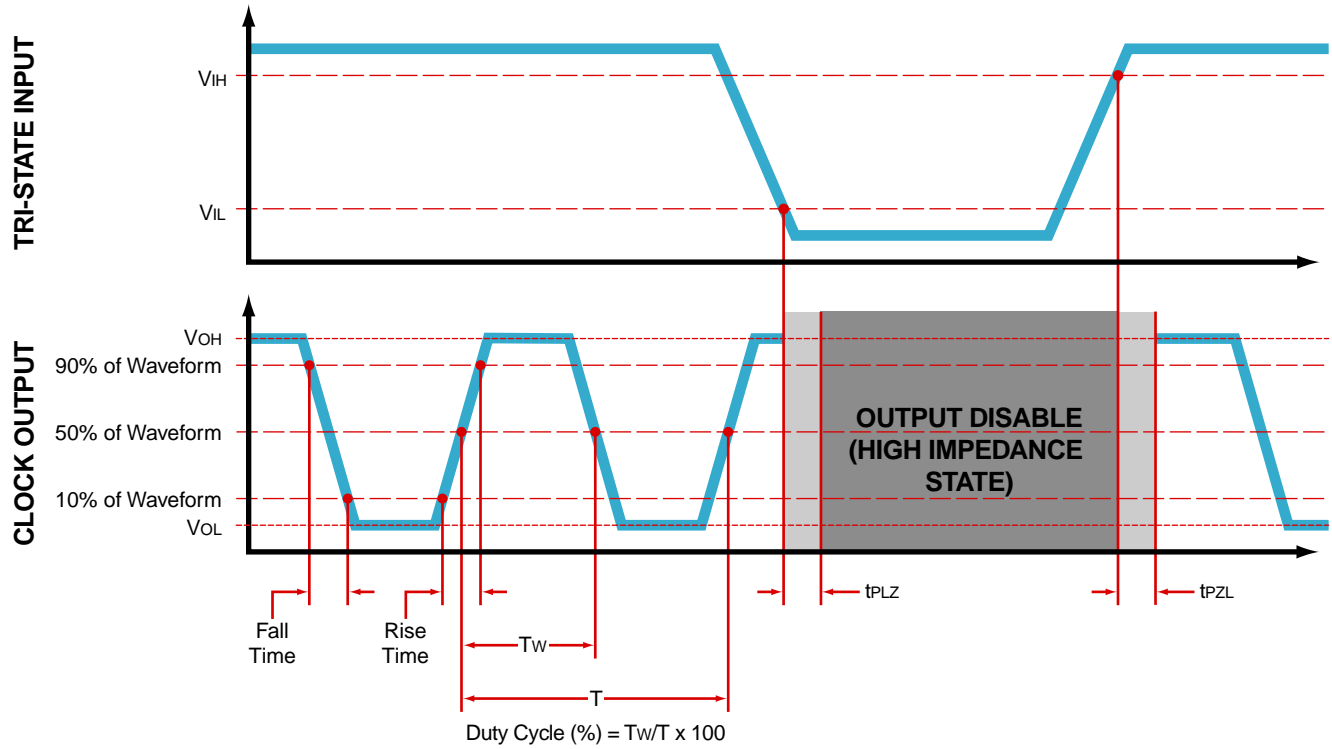
All Dimensions in Millimeters



All Tolerances are ±0.1

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## OUTPUT WAVEFORM & TIMING DIAGRAM



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## Test Circuit for CMOS Output



Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low input capacitance (<12pF), 10X Attenuation Factor, High Impedance (>10Mohms), and High bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value  $C_L$  includes sum of all probe and fixture capacitance. See applicable specification sheet for 'Load Drive Capability'.