

EQUA13C1E5-16.000M

[Click part number to visit Part Number Details page](#)

REGULATORY COMPLIANCE (Data Sheet downloaded on Mar 28, 2020)



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ITEM DESCRIPTION

Temperature Compensated Voltage Controlled Quartz Crystal Clock Oscillators TCVCXO LVCMOS (CMOS) 3.3Vdc 4 Pad 5.0mm x 7.0mm Ceramic Surface Mount (SMD) 16.000MHz 0°C to +50°C

ELECTRICAL SPECIFICATIONS

Nominal Frequency	16.000MHz
Frequency Stability	±3.0ppm Maximum (Inclusive of Operating Temperature Range, at Vdd=3.3Vdc, at Vc=1.5Vdc)
Frequency Stability vs. Frequency Tolerance	±2.0ppm Maximum (at 25°C ±2°C, at Vdd=3.3Vdc, at Vc=1.5Vdc)
Frequency Stability vs. Input Voltage	±0.2ppm Maximum (±5%)
Frequency Stability vs. Load	±0.2ppm Maximum (±2pF)
Frequency Stability vs. Reflow	±1.0ppm Maximum (at 25°C, 1 hour after reflow, 1 time)
Frequency Stability vs. Aging	±1ppm/Year Maximum (at 25°C)
Operating Temperature Range	0°C to +50°C
Supply Voltage	3.3Vdc ±5%
Input Current	10mA Maximum
Output Voltage Logic High (Voh)	90% of Vdd Minimum (IOH = -4mA)
Output Voltage Logic Low (Vol)	10% of Vdd Maximum (IOL = +4mA)
Rise/Fall Time	3nSec Maximum (Measured at 20% to 80% of waveform)
Duty Cycle	50 ±10(%) (Measured at 50% of waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Control Voltage	1.5Vdc ±1.0Vdc
Frequency Deviation	±5ppm Minimum
Linearity	10% Maximum
Transfer Function	Positive Transfer Characteristic
Modulation Bandwidth	10kHz Minimum (Measured at -3dB)
Input Impedance	1MOhms Minimum
Phase Noise	All Values are Typical -96dBc at 10Hz Offset -120dBc at 100Hz Offset -135dBc at 1kHz Offset -142dBc at 10kHz Offset -143dBc at 100kHz Offset -149dBc at 1MHz Offset -150dBc at 10MHz Offset -154dBc at 20MHz Offset
RMS Phase Jitter	1pSec Maximum (Fj=12kHz to 20MHz (Random))
Start Up Time	5mSec Maximum
Storage Temperature Range	-40°C to +85°C

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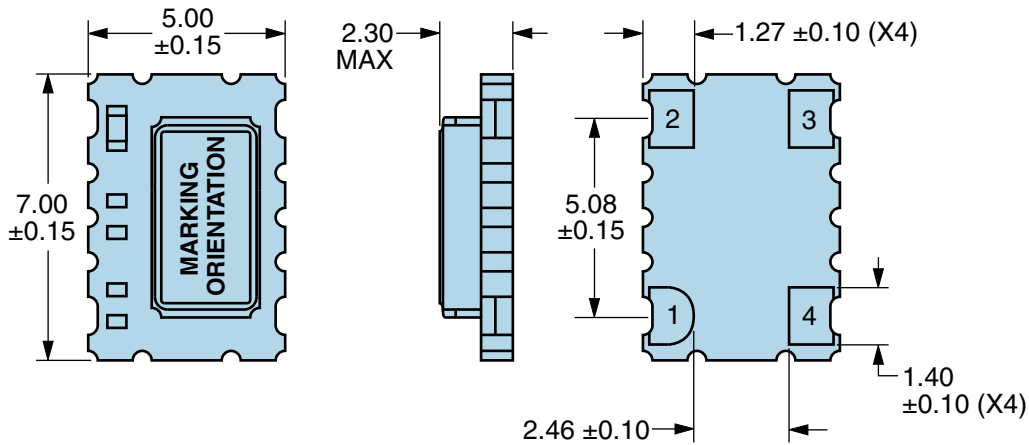
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ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

ESD Susceptibility	MIL-STD-883, Method 3015, Class 1, HBM: 1500V
Fine Leak Test	MIL-STD-883, Method 1014, Condition A
Flammability	UL94-V0
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Moisture Resistance	MIL-STD-883, Method 1004
Moisture Sensitivity	J-STD-020, MSL 1
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A

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MECHANICAL DIMENSIONS (all dimensions in millimeters)

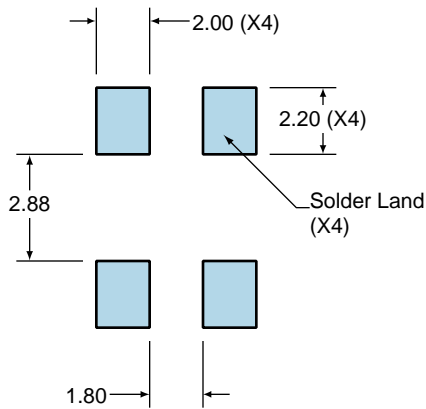


PIN	CONNECTION
1	Control Voltage
2	Case/Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	E16.000 E=Ecliptek Designator
2	XXXXX XXXXX=Ecliptek Manufacturing Identifier

Suggested Solder Pad Layout

All Dimensions in Millimeters

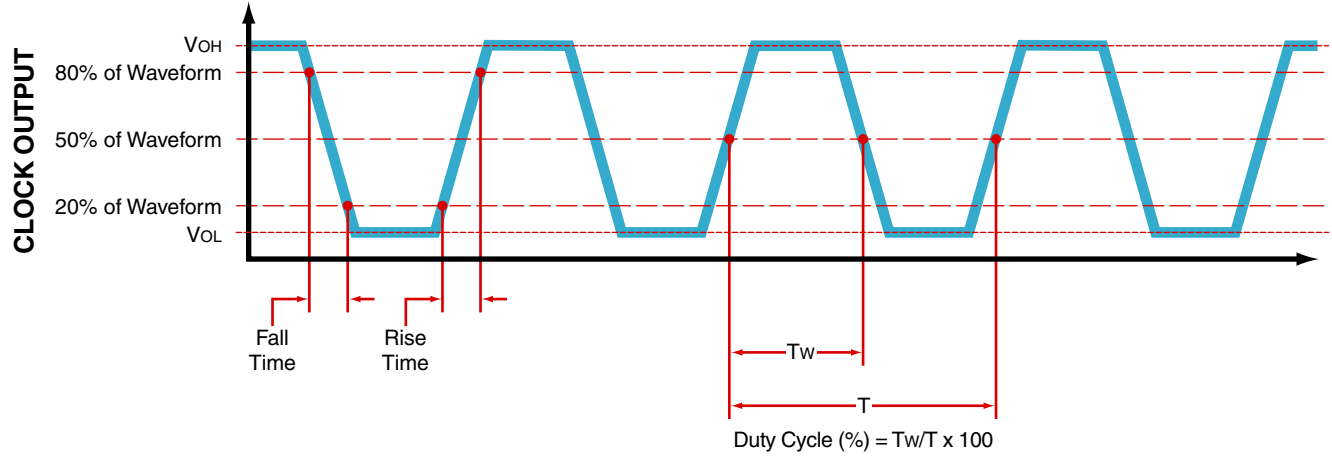


All Tolerances are ± 0.1

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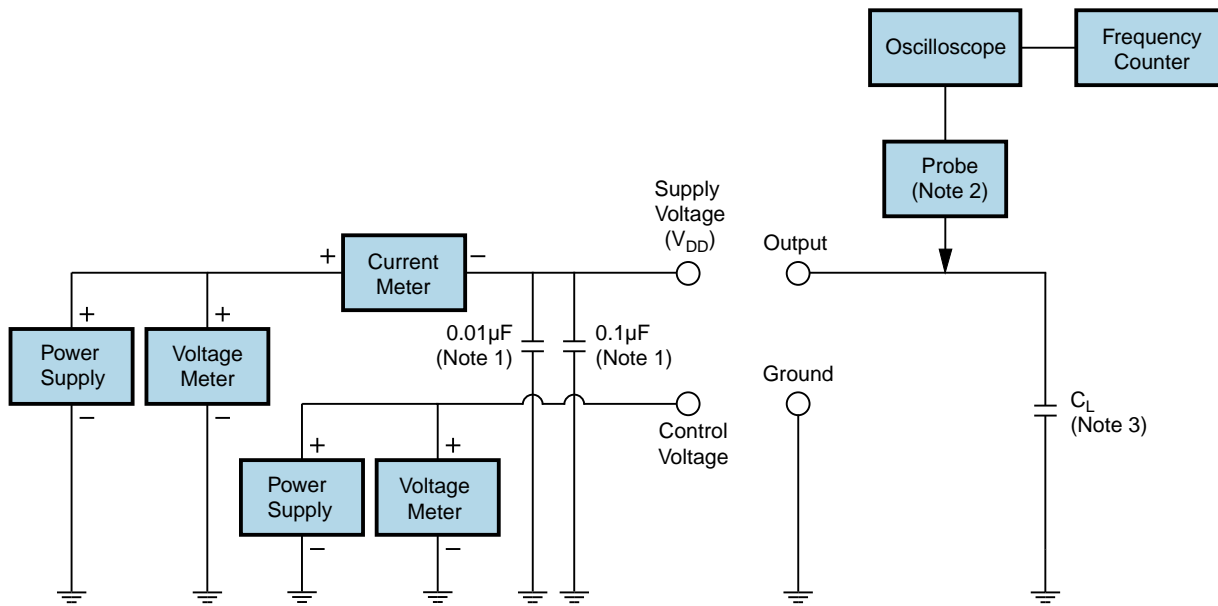
OUTPUT WAVEFORM



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Test Circuit for Voltage Control Option



Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.